16-Parameter LIST Module + 16-input PHA Module

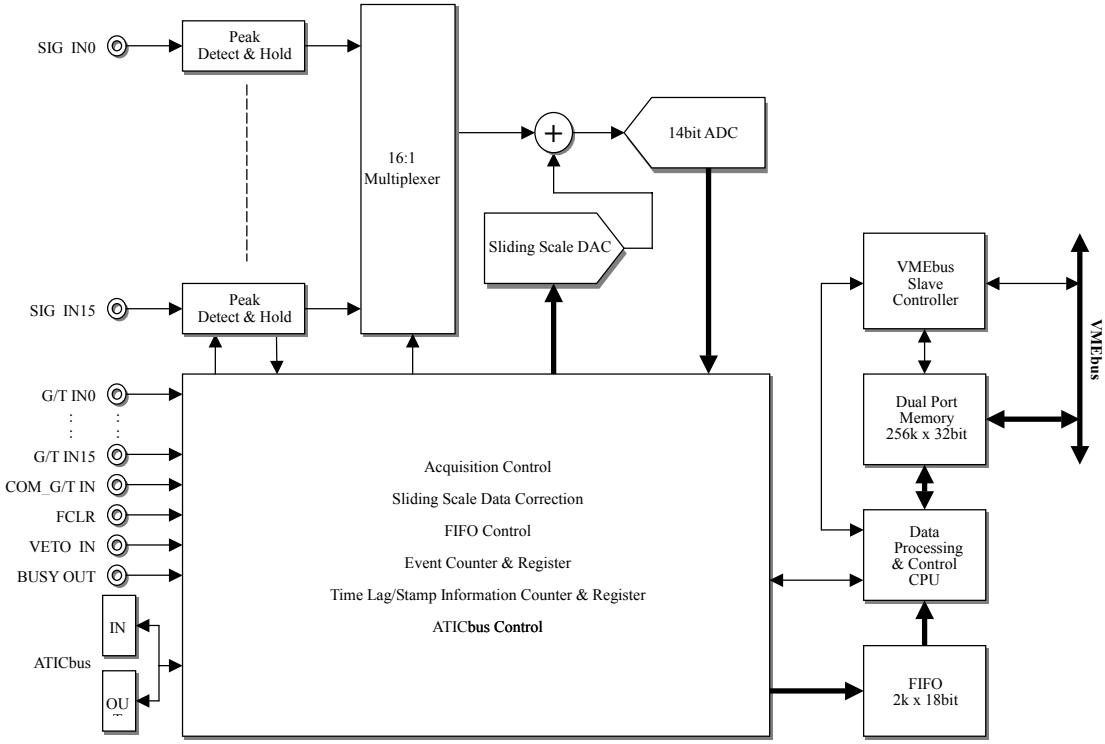
Model *A3100 (VME 6U)*

IWATSU RTT Model A3100 is 16 channel input LIST and PHA module. LIST, PHA or, both measurement modes are selectable. In front-end, high-speed peak detection and hold are implemented. Followed by multiplexer, 14bit ADC will converts peak heights. High performance ADC achieved INL < +/- 0.025% and DNL < +/- 1.0% for 99% full scale. The conversion time is 500nS.

Model A3100 can meet multiple applications with multiple timing modes. Since LIST function collects all events in all channels, Model A3100 is ideally suited for timing critical successive event data acquisition.

Model A3100 equipped 32 x 246k depth FIFO. This FIFO allows us to make seamless measurement. No dead time can be achieved during the data acquisition. Multi module operation is also achievable by ATICbus.

Block Diagram



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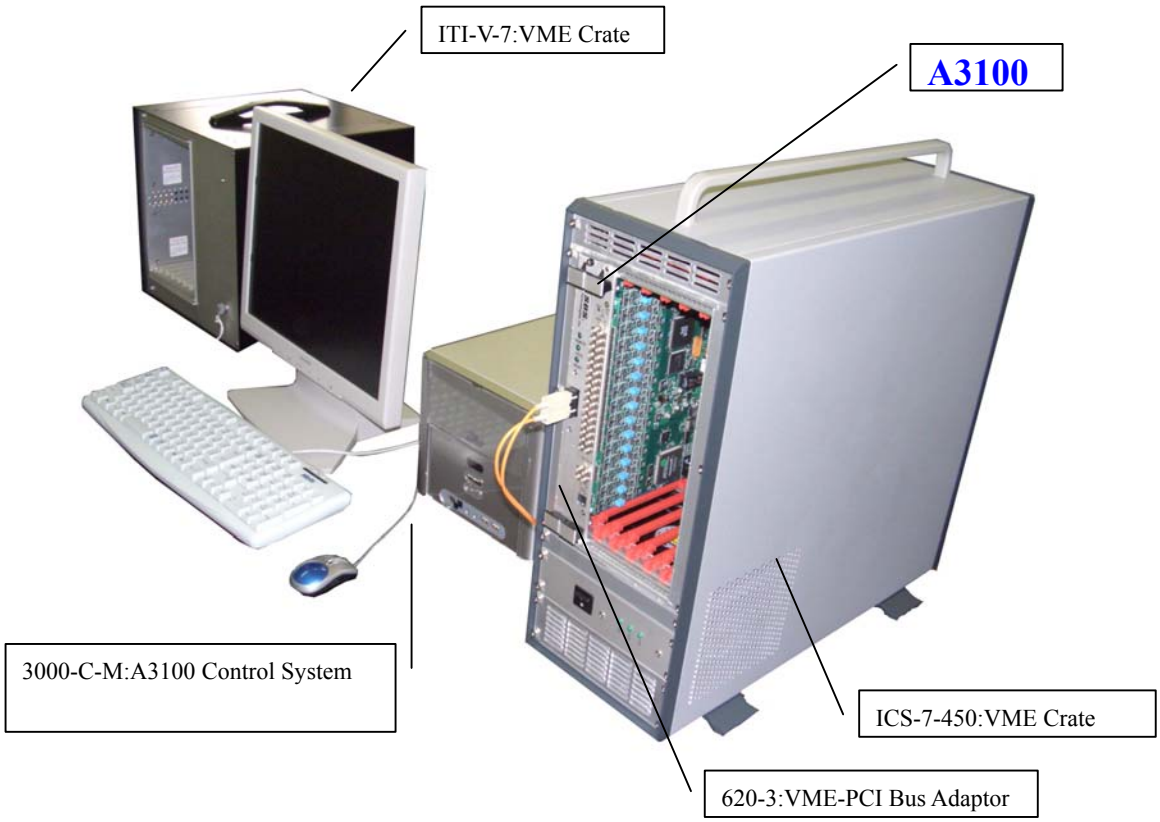
Example



LIST Measurement :

Three types of LIST measurement mode are available. Free-run LIST mode collects all event timing data. Gate LIST mode only collects data during the common gate signal is applied. And Triggered LIST mode collets other event timing data respect to the triggered signal. Collected data will show Event channel, ADC peak value, Time stamp. Since all data has a tag for the time information, it is quite easy to know the event-to-event time relation. If you are interested in only successive events, unwanted data can be eliminated from arbitrary time window. Utilizing the timing information, time-to-time spectrum growth can be monitored.

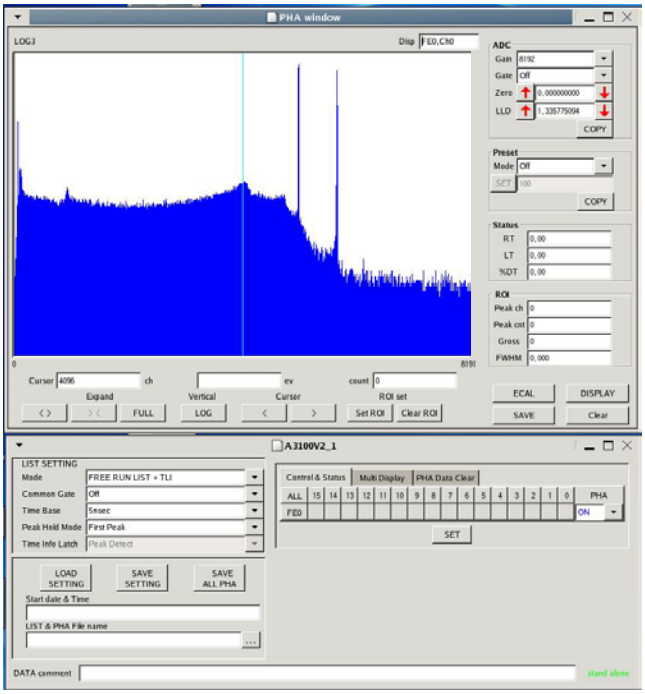
Left side data shows actual readout data from A3100. Each line indicates one event.
In first line,

- 0 : the index of A3100
- 1 : channel number
- 2665 : PHA ADC data
- 1025 : Time stamp clock. 1025 th clock
- 0 : Flipbit. Detection of coincidence in TLI mode

基準クロック	ｸﾛｯｸﾘｾｯﾄ時間
5ns	1.52hrs
10ns	3.05hrs
20ns	6.10hrs
50ns	15.2hrs
100ns	30.5hrs
200ns	2.5days
500ns	6.3days
1μs	12.7days

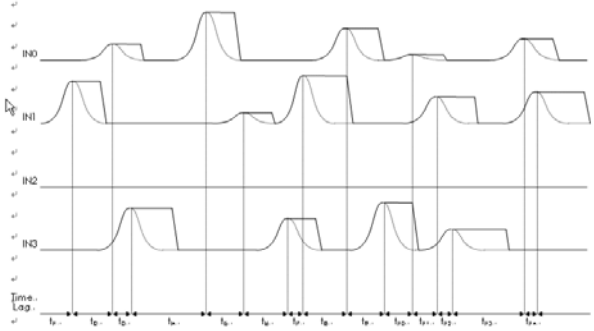
A3100 has 40bits roll-over event counter. The base clock can be selected from 5nS to 1uS. The table shows base clock and roll-over time.

Control Program

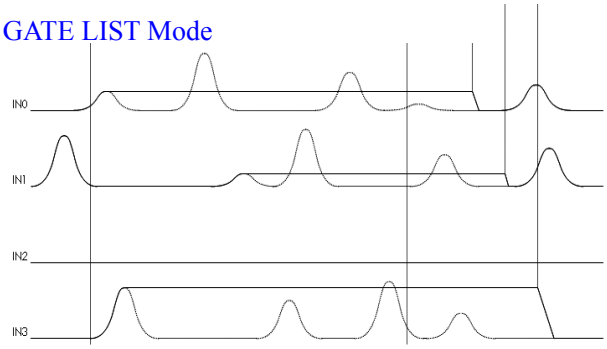


Control program runs on Linux. The program will control setting parameter in each channel, control acquisition and, manage the data. You can monitor the growth of spectrum in real time. It also has function to convert from channel scale to energy scale.

FREE RUN Mode



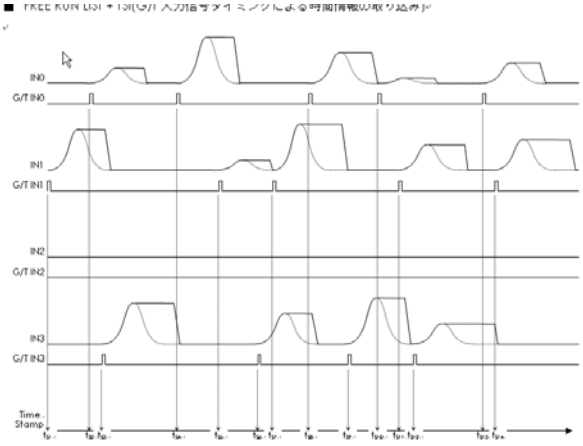
GATE LIST Mode



In Gate LIST mode, event data will be collected for only common gate was applied. Target channels are selectable.

Figure shows timing relation for each mode. Besides standard time stamp information (TSI), timing respect to the triggered event, time lag information (TLI) is also available. Latter data format easily allows to set reasonable time window to eliminate unwanted event data. Basic clock for TSI and TLI can be selected from 5nS up to 1uS.

Triggered LIST Mode



Arbitrary channel can be selected to trigger the timing measurement. Event timing data will be recorded respect to the each triggered signal.

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Specification	·
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SIG IN	16 channel input, 0-10V positive unipolar pulse, Minimum rise time: 200nS, Minimum pulse width : 500nS Zin 1k Ohm, LEMO connector
ZERO ADJUST	Each channel employs 12bit DAC, which 5% of full scale input can be adjusted.
LLD	10% of full scale input can be adjusted by 12 bit DAC
ADC GAIN Select	256/512/1024/2048/4096/8192 programmable for each channel
Conversion time	500nS (from peak detection to completion of writing FIFO
Integration non-linearlity	< +/- 0.025% out of 99% of the full scale
Differentiation non-linearlity	< +/- 1.0% out of 99% of the full scale
Measurement mode	Selectable measurement mode PHA, Gated LIST, Free run LIST, Triggered LIST PHA and LSIT mode measurement simultaneously Gated LIST and Triggered LIST mode·
Data Memory	256k×32bit Dual Port Memory 32bit x 256k depth FIFO PHA mode 8kch x 32bit x 16ch data memory LIST mode 127k x 32bit Register 1k x 32bit
PHA mode preset conditions	Selectable options for each channel Real time: Off, 42949672 sec Live time: Off, 42949672 sec Peak counts: Off, 4294967 Area counts: Off, 4294967
LIST buffer preset	Notify user when the number of event hit exceed preset LIST data size or the preset number of event count.
Real & Live Time	Minimum measurable count time: 10mS
Event Counter	28bit event counter with COM_GT IN (Common Gate trigger) is utilized
TLI/TSI Counter	Time stamp counter 40bits for TLI/TSI measurement Time base 5nS/10nS/20nS/50nS/100nS/200nS/500nS/1uS
TLI/TSI data	Maximum time resolution: 5nS MCSR register time base：5ns

Throughput	PHA: 205kcps Free run LIST + TSI/TLI: 109kcps Triggered LIST + TSI/TLI: 72kcps Gated LSIT: 98/selected cahnnels + 5 kcps PHA + LIST simultaneous : (P x L)/(P + L) kcps P: throughput for PHA mode L: thorughput for LIST mode
Fast Clear time	Maximum 600nS
Control signal input	Gate/Trigger Input 0-15 channal: TTL, LEMO connector Common gate/ trigger : TTL, LEMO connector FCLR In, clear peak hold : TTL, LEMO connector VETO Input, veto ADC activity, TTL, LEMO connectorG/T IN0 – 15
Control signal out	Busy signal, FIFO full: TTL, LEMO connector
ATIC Bus In/Out	Acquisition and Time information Control Bus When mutiple A3100 modules were employed, this bus controls all modules.
VME Bus Interface	A24/A32 address mode, D16/D32/BLT data transfer, MCST 6U1W VME module
Power	+5V/0.85A、+12V/0.85A、-12V/0.9A

Contact
Satoshi Hayakawa
Riverside Trade and Technology
6101 Quail Valley Court, A106
Riverside CA 92507
Phone 951-347-2008
Mail: Sales@riversidetnt.com

Jun Saito: jun.saito@iwatsu.co.jp
7-41, Kugayama 1 Chome, Suginami-ku, Tokyo 168-8511
TEL 03-3335-2121 FAX 03-3335-2010
URL: http://www.iti.iwatsu.co.jp/

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